




INTEGRATED CIRCUIT COMPUTING DEVICE COMPRISING DYNAMICALLY CONFIGURABLE GATE ARRAY HAVING A RECONFIGURABLE EXECUTION MEANS

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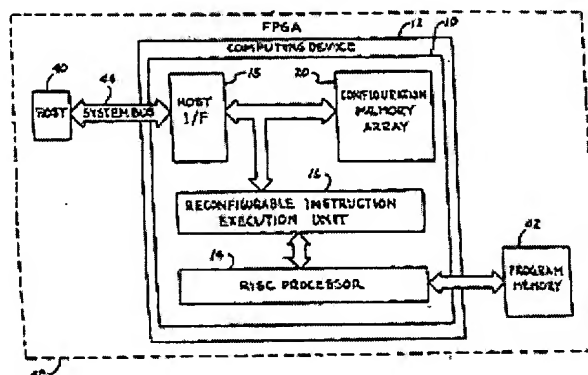
 EP0626084 (A1)
 US5361373 (A1)
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Cited documents:

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Abstract of WO9414123

An integrated circuit computing device (10) is comprised of a dynamically configurable Field Programmable Gate Array (FPGA) (12). This gate array (12) is configured to implement a RISC processor (14) and a Reconfigurable Instruction Execution Unit (16). Since the FPGA (12) can be dynamically reconfigured, the Reconfigurable Instruction Execution Unit (16) can be dynamically changed to implement complex operations in hardware rather than in time-consuming software routines. This feature allows the computing device (10) to operate at speeds that are orders of magnitude greater than traditional RISC or CISC counterparts. In addition, the programmability of the computing device (10) makes it very flexible and hence, ideally suited to handle a large number of very complex and different applications.



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<p>(21) International Application Number: PCT/US93/11964 (22) International Filing Date: 9 December 1993 (09.12.93) (30) Priority Data: 07/989,236 11 December 1992 (11.12.92) US (71) Applicant: NATIONAL TECHNOLOGY, INC. [US/US]; Suite 400, 2835 Hollywood Avenue, Shreveport, LA 71108 (US). (72) Inventor: GILSON, Kent, L.; Apartment 120, 255 North Main Street, Salt Lake City, UT 84115 (US). (74) Agent: WEISS, Harry, M.; Harry M. Weiss & Associates, 4204 North Brown Avenue, Scottsdale, AZ 85251 (US).</p>		<p>(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>

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